What is claimed is:

1. A method for writing data in a memory array, the method comprising:

(a) providing a memory device comprising a memory array comprising a plurality of groups of sub-arrays and further comprising a register storing a value N representing a number of groups of sub-arrays into which data will be simultaneously written;

(b) changing the value stored in the register from N to M; and

(c) simultaneously writing data into M groups of sub-arrays.

2. The invention of Claim 1 further comprising:

(d) changing the value stored in the register from M to L; and

(e) simultaneously writing data into L groups of sub-arrays.

3. The invention of Claim 1, wherein N comprises a default value.

4. The invention of Claim 1, wherein (b) is performed in response to a signal from a host device coupled with the memory device.

5. The invention of Claim 1, wherein (b) is performed in response to a command issued by a user of a host device coupled with the memory device.

6. The invention of Claim 1, wherein (b) is performed in response to a signal from temperature-based control circuitry.

7. The invention of Claim 1, wherein (b) is performed during testing of the memory array.

8. The invention of Claim 1, wherein the memory array comprises a three-dimensional memory array.

9. The invention of Claim 1, wherein the memory array comprises a plurality of antifuse memory cells.

10. The invention of Claim 1, wherein the memory array comprises a plurality of write-once memory cells.

11. The invention of Claim 1, wherein the memory array comprises a plurality of write-many memory cells.

12. A method for reading data from a memory array, the method comprising:

(a) providing a memory device comprising a memory array comprising a plurality of groups of sub-arrays and further comprising a register storing a value N representing a number of groups of sub-arrays from which data will be simultaneously read;

(b) changing the value stored in the register from N to M; and

(c) simultaneously reading data from M groups of sub-arrays.

13. The invention of Claim 12 further comprising:

(d) changing the value stored in the register from M to L; and

(e) simultaneously reading data from L groups of sub-arrays.

14. The invention of Claim 12, wherein N comprises a default value.

15. The invention of Claim 12, wherein (b) is performed in response to a signal from a host device coupled with the memory device.

16. The invention of Claim 12, wherein (b) is performed in response to a command issued by a user of a host device coupled with the memory device.

17. The invention of Claim 12, wherein (b) is performed in response to a signal from temperature-based control circuitry.

18. The invention of Claim 12, wherein (b) is performed during testing of the memory array.

19. The invention of Claim 12, wherein the memory array comprises a three-dimensional memory array.

20. The invention of Claim 12, wherein the memory array comprises a plurality of antifuse memory cells.

21. The invention of Claim 12, wherein the memory array comprises a plurality of write-once memory cells.

22. The invention of Claim 12, wherein the memory array comprises a plurality of write-many memory cells.

23. A memory device comprising:

a memory array comprising a plurality of groups of sub-arrays;

a register; and

circuitry operative to simultaneously write data into N number of groups of sub-arrays, wherein N is a value stored in the register.

24. The invention of Claim 23, wherein N is a default value for the register.

25. The invention of Claim 23, wherein the memory device is coupled with a host device, and wherein N is stored in the register by the host device.

26. The invention of Claim 23 further comprising temperature-based control circuitry

coupled with the register, and wherein N is stored in the register by the temperature-based control circuitry.

27. The invention of Claim 23 further comprising:

a plurality of data registers coupled with the plurality of groups of sub-arrays;

register selection logic coupled with the plurality of data registers and the register; and

sub-array group selection logic coupled with the plurality of groups of sub-arrays and the register.

28. The invention of Claim 23 further comprising:

a data register comprising a plurality of register ports coupled with the plurality of groups of sub-arrays;

port control logic coupled with the plurality of registers ports and the register; and

sub-array group selection logic coupled with the plurality of groups of sub-arrays and the register.

29. The invention of Claim 23 further comprising:

a data register;

a variable serial-to-parallel connection circuit, the variable serial-to-parallel connection circuit coupled with the register and coupling the data register to the plurality of groups of sub-arrays; and

sub-array group selection logic coupled with the plurality of groups of sub-arrays and the register.

30. The invention of Claim 23, wherein the memory array comprises a three-dimensional memory array.

31. The invention of Claim 23, wherein the memory array comprises a plurality of antifuse memory cells.

32. The invention of Claim 23, wherein the memory array comprises a plurality of write-once memory cells.

33. The invention of Claim 23, wherein the memory array comprises a plurality of write-many memory cells.

34. A method for writing data in a memory array, the method comprising:

(a) providing a memory array comprising a plurality of groups of sub-arrays;

(b) storing a value N representing a number of groups of sub-arrays into which data will be simultaneously written;

(c) changing the stored value from N to M; and

(d) simultaneously writing data into M groups of sub-arrays.

35. The invention of Claim 34, wherein the memory array is part of a memory device comprising a register, and wherein the value is stored in the register.

36. The invention of Claim 34, wherein the value is stored in the memory array.

37. The invention of Claim 34, wherein the memory array is part of a memory device coupled with a host device, and wherein the value is stored in the host device.

38. The invention of Claim 34, wherein the memory array comprises a three-dimensional memory array.

39. The invention of Claim 34, wherein the memory array comprises a plurality of antifuse memory cells.

40. The invention of Claim 34, wherein the memory array comprises a plurality of write-once memory cells.

41. The invention of Claim 34, wherein the memory array comprises a plurality of write-many memory cells.

42. A method for writing data in a passive-element memory array, the method comprising:

(a) providing a passive-element memory array comprising a plurality of groups of sub-arrays;

(b) selecting a number of groups of sub-arrays fewer than all of the groups into which data will be simultaneously written; and

(c) simultaneously writing data into the selected number of groups of sub-arrays.

43. The invention of Claim 42, wherein each group of sub-arrays comprises a respective plurality of sub-arrays, and wherein (c) comprises simultaneously writing data into fewer than all of the sub-arrays in each of the selected number of groups of sub-arrays.

44. The invention of Claim 42, wherein each group of sub-arrays comprises a respective plurality of sub-arrays, and wherein (c) comprises simultaneously writing data into all of the sub-arrays in each of the selected number of groups of sub-arrays.

45. The invention of Claim 42, wherein each group of sub-arrays comprises a respective plurality of sub-arrays, and wherein (c) comprises simultaneously writing data into only one sub-array in each of the selected number of groups of sub-arrays.

46. The invention of Claim 42, wherein each group of sub-arrays comprises a respective plurality of sub-arrays, and wherein all of the sub-arrays in each respective group share a respective data bus.

47. The invention of Claim 46, wherein (c) comprises simultaneously writing data into fewer than all of the sub-arrays in each of the selected number of groups of sub-arrays.

48. The invention of Claim 47, wherein (c) comprises simultaneously writing data into only one sub-array in each of the selected number of groups of sub-arrays.

49. The invention of Claim 42, wherein each group of sub-arrays comprises a respective plurality of sub-arrays, and wherein (c) comprises simultaneously writing data into the same number of sub-arrays in each group.

50. The invention of Claim 42, wherein each group of sub-arrays comprises a respective plurality of sub-arrays, and wherein all of the sub-arrays are written into when writing a page of data.

51. The invention of Claim 42, wherein the selected number of groups of sub-arrays is stored in a register.

52. The invention of Claim 51, wherein the register stores a default value, and wherein the default value is overwritten by the selected number of groups of sub-arrays.

53. The invention of Claim 42, wherein the number of groups of sub-arrays is automatically selected by a host device coupled with the memory array.

54. The invention of Claim 42, wherein the number of groups of sub-arrays is manually selected by a user of a host device coupled with the memory array.

55. The invention of Claim 42, wherein the number of groups of sub-arrays is automatically selected by temperature-based control circuitry.

56. The invention of Claim 42, wherein the number of groups of sub-arrays is selected during testing of the memory array.

57. The invention of Claim 42, wherein the memory array comprises a three-dimensional memory array.

58. The invention of Claim 42, wherein the memory array comprises a plurality of antifuse memory cells.

59. The invention of Claim 42, wherein the memory array comprises a plurality of write-once memory cells.

60. The invention of Claim 42, wherein the memory array comprises a plurality of write-many memory cells.

61. A method for writing data in a write-once memory array, the method comprising:

(a) providing a write-once memory array comprising a plurality of groups of sub-arrays;

(b) selecting a number of groups of sub-arrays fewer than all of the groups into which data will be simultaneously written; and

(c) simultaneously writing data into the selected number of groups of sub-arrays.

62. The invention of Claim 61, wherein (b) is performed in user mode and not in test mode.

63. The invention of Claim 61, wherein the selected number of groups of sub-arrays is stored in a register.

64. The invention of Claim 63, wherein the register stores a default value, and wherein the default value is overwritten by the selected number of groups of sub-arrays.

65. The invention of Claim 61, wherein the number of groups of sub-arrays is automatically selected by a host device coupled with the memory array.

66. The invention of Claim 61, wherein the number of groups of sub-arrays is manually selected by a user of a host device coupled with the memory array.

67. The invention of Claim 61, wherein the number of groups of sub-arrays is automatically selected by temperature-based control circuitry.

68. The invention of Claim 61, wherein the number of groups of sub-arrays is selected during testing of the memory array.

69. The invention of Claim 61, wherein the memory array comprises a three-dimensional memory array.

70. The invention of Claim 61, wherein the memory array comprises a plurality of antifuse memory cells.

71. A method for writing data in a memory array used in a host device, the method comprising:

(a) providing a host device coupled with a memory device comprising a memory array comprising a plurality of groups of sub-arrays;

(b) selecting a number of groups of sub-arrays fewer than all of the groups into which data will be simultaneously written; and

(c) simultaneously writing data into the selected number of groups of sub-arrays.

72. The invention of Claim 71, wherein the selected number of groups of sub-arrays is stored in a register in the memory device.

73. The invention of Claim 72, wherein the register stores a default value, and wherein the default value is overwritten by the selected number of groups of sub-arrays.

74. The invention of Claim 71, wherein (b) is performed in user mode and not in test mode.

75. The invention of Claim 71, wherein (b) is performed in the field.

76. The invention of Claim 75, wherein (b) is performed in the field in response to a signal from the host device.

77. The invention of Claim 75, wherein (b) is performed in the field in response to a command issued by a user of the host device.

78. The invention of Claim 75, wherein (b) is performed in the field in response to a signal from temperature-based control circuitry in the memory device.

79. The invention of Claim 71, wherein the memory array comprises a three-dimensional memory array.

80. The invention of Claim 71, wherein the memory array comprises a plurality of antifuse memory cells.

81. The invention of Claim 71, wherein the memory array comprises a plurality of write-once memory cells.

82. The invention of Claim 71, wherein the memory array comprises a plurality of write-many memory cells.

83. A method for writing data in a write-once passive-element memory array, the method comprising:

(a) providing a host device coupled with a memory device comprising a write-once passive-element memory array comprising a plurality of groups of sub-arrays, each group of sub-arrays comprising a respective plurality of sub-arrays sharing a respective data bus;

(b) storing in a register a selected number of groups of sub-arrays fewer than all of the groups into which data will be simultaneously written; and

(c) simultaneously writing data into fewer than all the sub-arrays in each of the selected number of groups of sub-arrays.

84. The invention of Claim 83, wherein (c) comprises simultaneously writing data into only one sub-array in each of the selected number of groups of sub-arrays.

85. The invention of Claim 83, wherein (b) is performed in the field.

86. The invention of Claim 85, wherein (b) is performed in the field in response to a signal from the host device.

87. The invention of Claim 85, wherein (b) is performed in the field in response to a command issued by a user of the host device.

88. The invention of Claim 85, wherein (b) is performed in the field in response to a signal from temperature-based control circuitry in the memory device.

89. The invention of Claim 83, wherein the memory array comprises a three-dimensional memory array.

90. The invention of Claim 83, wherein the memory array comprises a plurality of antifuse memory cells.